Midterm Exam

(February 18th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (20 PTS)

a) Complete the following table. The decimal numbers are unsigned: (6 pts.)

Decimal	BCD	Binary	Reflective Gray Code
97			
			101010
		1100010	
	000101010110		

b) Complete the following table. Use the fewest number of bits in each case: (12 pts.)

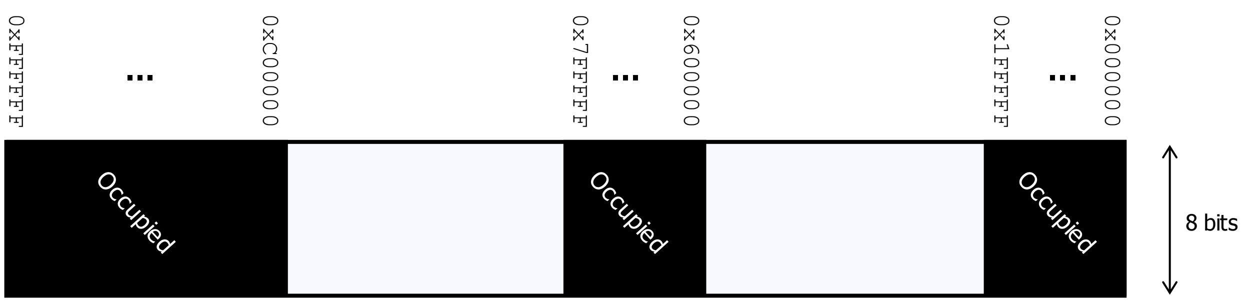
	REPRESENTATION		
Decimal	**Sign-and-magnitude**	**1's complement**	**2's complement**
			100000
	11001100		
		1011110	
		01000101	
-64			
			101101

c) Convert the following decimal numbers to their 2's complement representations. (2 pts)

- ✓ -31.3125
- ✓ 17.375

PROBLEM 2 (10 PTS)

- The figure below depicts the entire memory space of a microprocessor. Each memory address occupies one byte. 1KB = 2^{10} bytes, 1MB = 2^{20} bytes, 1GB = 2^{30} bytes
  - ✓ What is the size (in bytes, KB, or MB) of the memory space? What is the address bus size of the microprocessor?
  - ✓ If we have a memory chip of 2 MB, how many bits do we require to address those 2 MB of memory?
  - ✓ We want to connect the 2 MB memory chip to the microprocessor. The figure shows all the occupied portions of the memory space. Provide an address range so that 2 MB of memory is properly addressed. You can only use the non-occupied portions of the memory space as shown in the figure below.



PROBLEM 3 (12 PTS)

- Given two 4-bit <u>unsigned</u> numbers A, B, sketch the circuit that computes $|A - B| \times 4$. For example: $A = 0011, B = 1010 \rightarrow |A - B| = 7$, $|A - B| \times 4 = 28$. You can only use full adders and logic gates. Make sure your circuit avoids overflow.

PROBLEM 4 (18 PTS)

a) Perform the following additions and subtractions of the following unsigned integers. Use the fewest number of bits n to represent both operators. Indicate every carry (or borrow) from c_0 to c_n (or b_0 to b_n). For the addition, determine whether there is an overflow. For the subtraction, determine whether we need to keep borrowing from a higher byte. (6 pts)

- ✓ 51 + 27
- ✓ 19 - 42

b) Perform the following operations, where numbers are represented in 2's complement. Indicate every carry from c_0 to c_n. For each case, use the fewest number of bits to represent the summands and the result so that overflow is avoided. (8 pts)

- ✓ 127 - 76
- ✓ -69 - 97

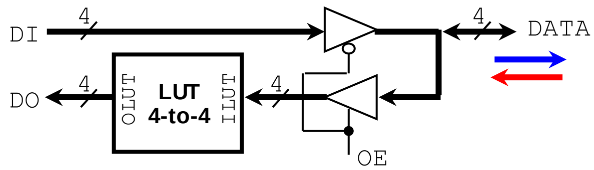
c) Get the multiplication result of the following numbers that are represented in 2's complement arithmetic with 4 bits. (4 pts)

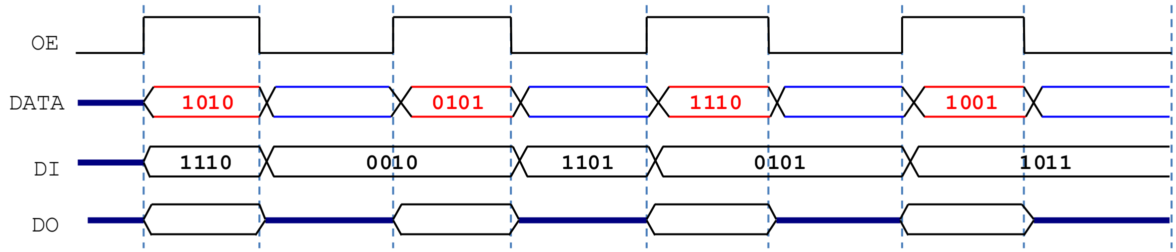
- ✓ -7 x 5.

PROBLEM 5 (10 PTS)

- Given the following circuit, complete the timing diagram (signals DO and $DATA$).
  The LUT 4-to-4 implements the following function: $OLUT = \lfloor sqrt(ILUT) \rfloor$. For example: $ILUT = 1100 \rightarrow OLUT = 0100$

Input data to LUT is treated as an unsigned number.

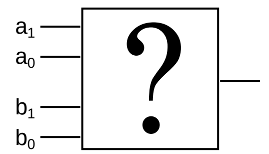




PROBLEM 6 (15 PTS)

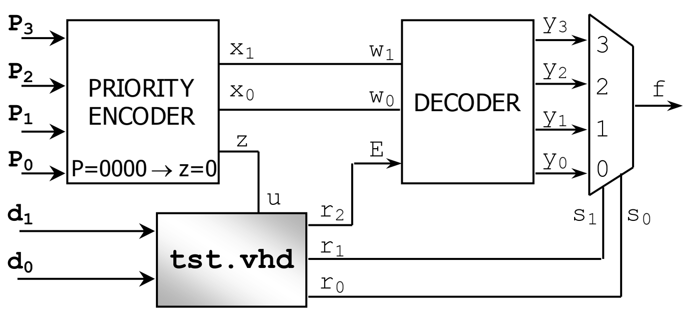
a) We want to design a circuit that determines whether two 2-bit numbers $A = a_1a_0, B = b_1b_0$ are equal: $f = 1\ if\ A = B, f = 0\ if\ A \neq B$. Sketch this circuit using logic gates. (4 pts)

b) Implement the previous circuit using <u>ONLY</u> 2-to-1 MUXs (AND, OR, NOT, XOR gates are not allowed). (11 pts)



PROBLEM 7 (15 PTS)

- Complete the timing diagram of the following circuit. The VHDL code (`tst.vhd`) corresponds to the shaded circuit.
  $d = d_1d_0$, $w = w_1w_0$, $r = r_2r_1r_0$, $y = y_3y_2y_1y_0$




```
library ieee;
use ieee.std_logic_1164.all;
entity tst is
  port (d: in std_logic_vector(1 downto 0);
        r: out std_logic_vector(2 downto 0);
        u: in std_logic);
end tst;
```

```
architecture bhv of tst is

begin

  process (d, u)
  begin

     r <= '0'&d;
     if u = '1' then
        r <= d&'1';
     end if;

  end process;

end bhv;
```